i,

PATENT ABSTRACTS OF JAPAN

(11)Publication number:

09-081615

(43) Date of publication of application: 28.03.1997

(51)Int.CI.

G06F 17/50

G06F 15/18

(21)Application number: 07-236512

(71)Applicant: SONY CORP

(22)Date of filing:

14.09.1995

(72)Inventor: KITANO HIROAKI

(54) CIRCUIT DESIGNING DEVICE AND METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To design a large scale

logic circuit.

SOLUTION: Based on genetic algorithm, the circuit constitution of a programmable logic circuit (PLD) is updated and the logic circuit for performing object output is designed. Corresponding to the genetic algorithm, the set of grammatical rules (for instance,

 $\langle a \rangle \qquad \qquad A \rightarrow \begin{bmatrix} O & C \\ H & L \end{bmatrix}$

output is designed. Corresponding to the genetic algorithm, the set of grammatical rules (for instance, (a) to (d)) for leading out the circuit constitution of the PLD

(b) F→ L H

is turned to a chromosome, the chromosome (the set of the grammatical rules) is updated and the chromosome for supplying optimum circuit constitution is led out. At

(e) H - ☐ (T Q)

the time, since the length of the chromosome is proportional to the number of the grammatical rules, without depending on the scale of the circuit of the PLD,

(q), $O \Rightarrow \begin{bmatrix} 1 & E \\ O & O \end{bmatrix}$

the circuit constitution is designed in appropriate calculation time even when the circuit of the PLD is a large scale.

large scale.

LEGAL STATUS

[Date of request for examination]

17.09.2002

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

- JPO and NCIPI are not responsible for any damages caused by the use of this translation.
 - 1. This document has been translated by computer. So the translation may not reflect the original precisely.
 - 2.*** shows the word which can not be translated.
 - 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] Circuit design equipment characterized by having an operation means by which it can calculate and a calculation function can be changed dynamically, and the control means which changes said calculation function so that the output of said operation means may approach the output of the purpose based on the genetic algorithm which uses as a chromosome the syntax Ruhr which derives said calculation function.

[Claim 2] The circuit design approach characterized by changing said calculation function based on the genetic algorithm which uses the syntax Ruhr which derives said calculation function of the arithmetic element which calculates, and which can change a calculation function dynamically as a chromosome so that the result of said operation may approach the target value.

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.*** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the circuit design equipment and the approach of changing circuitry especially about circuit design equipment and an approach based on a genetic algorithm.

[0002]

[Description of the Prior Art] Conventionally, the designer was designing the logical circuit, combining many fundamental logical elements experientially, when the complicated logical circuit which controls a robot etc. was designed however, the method of designing a logical circuit recently based on a genetic algorithm (GA: Genetic Algorithm), without needing experiential knowledge — for example, Mr. Higuchi — ** — in "the genetic algorithm (volume for Hiroaki Kitano, Sangyo Tosho Publishing)", it is introduced as "a fundamental experiment of the hardware evolution by hereditary study."

[0003] In this approach, the circuitry of a programmable logical circuit (PLD: Programmable Logic Device) represented by FPGA (Field Programmable Gate Array) is repeatedly changed based on GA, and the logical circuit which outputs the purpose is created.

[0004] PLD has two or more logic cells which can choose dynamically the class of fundamental logistics, such as AND logical operation and OR logical operation, and can change the class of logistic which each logic cell performs, and the pattern of circuit association between these logic cells

[0005] In GA, what the object to optimize is characterized is expressed with a gene, it is connecting this gene and a chromosome is generated. And the object is brought close to the optimal condition by repeating and updating two or more chromosomes.

[0006] Conventionally, the function of the logic cell in PLD and the pattern of circuit association between logic cells are expressed in a chromosome, and update this chromosome (circuitry of PLD) based on GA, and it is made as [create / the logical circuit which outputs the purpose]. [0007]

[Problem(s) to be Solved by the Invention] However, when designing the logical circuit which performs complicated control, many logical operation components are needed and the joint pattern between these logical operation components also becomes complicated. In a Prior art, in order to express the function of a logic cell and the pattern of circuit association in PLD in a chromosome, the die length of a chromosome becomes long according to the number of logic cells. Therefore, since it is necessary to perform the operation based on GA to a very long chromosome when designing a large-scale logical circuit, it has the technical problem that much computation time is required.

[0008] This invention generates the function and joint pattern of a logic cell, and it is made not to depend for the die length of a chromosome on the number of logic cells, and it enables it to be the set of the syntax Ruhr which was made in view of such a situation and consists of a predetermined number of syntax Ruhr, and to design a large-scale logical circuit by expressing these syntax Ruhr in a chromosome.

[0009]

[Means for Solving the Problem] Circuit design equipment according to claim 1 calculates, and is characterized by having an operation means by which a calculation function can be changed dynamically, and the control means which changes a calculation function so that the output of an operation means may approach the output of the purpose based on the genetic algorithm which uses as a chromosome the syntax Ruhr which derives a calculation function.

[0010] Based on the genetic algorithm which uses the syntax Ruhr which derives said calculation function of the arithmetic element which calculates, and which can change a calculation function dynamically as a chromosome, the circuit design approach according to claim 2 is characterized by changing said calculation function so that the result of said operation may approach the target value.

[0011] In circuit design equipment according to claim 1, an operation means by which a calculation function can be changed dynamically calculates, and based on the genetic algorithm which uses as a chromosome the syntax Ruhr which derives a calculation function, a control means changes a calculation function so that the output of an operation means may approach the output of the purpose.

[0012] In the circuit design approach according to claim 2, based on the genetic algorithm which uses the syntax Ruhr which derives said calculation function of the arithmetic element which calculates, and which can change a calculation function dynamically as a chromosome, said calculation function is changed so that the result of said operation may approach the target value.

[0013]

[Embodiment of the Invention] <u>Drawing 1</u> shows the example of a configuration of one example of the circuit design equipment of this invention. This example of a configuration is equipped with PLD1 (operation means). It connects with an arithmetic unit 2 (control means), and PLD1 changes the circuitry according to the control signal of an arithmetic unit 2, is the circuitry and is made as [output / to a robot 11 / a control signal].

[0014] The robot 11 is made as [operate] according to the control signal supplied from PLD1. A designer 21 observes actuation of a robot 11, evaluates the actuation according to the predetermined evaluation approach (performance index), operates an input unit 3, and performs the input corresponding to the evaluation to an arithmetic unit 2.

[0015] An arithmetic unit 2 holds a predetermined number of chromosomes, from each chromosome, draws the circuitry of PLD1 and is made as [output / to PLD1 / as a control signal]. Moreover, about all chromosomes, after actuation of a robot 11 and evaluation of a designer 21 are completed, based on GA, an arithmetic unit 2 makes high the probability for many descendants to the next generation of the chromosome corresponding to the circuitry which realized actuation with high evaluation to remain, and is made as [update / a chromosome]. [0016] Drawing 2 shows the example of a configuration of PLD1. This example of a configuration is equipped with two or more logic cells 41–1 thru/or 41–N. These logic cells 41–1 thru/or 41–N have two or more fundamental logistic functions, such as AND logical operation and OR logical operation, and is made as [change / dynamically / according to the control signal supplied from the outside / the class of logistic to perform].

[0017] A logic cell 41-1 thru/or 41-N are made as [combine / every logic cells], and it is determined by the control signal supplied from the outside whether between each logic cell is combined. When combining between logic cells, the joint switch with which it corresponds of the joint switch 42-1 thru/or the 42-M is turned ON. For example, when combining logic-cell 41-N and a logic cell 41-1, the joint switch 42-1 is turned ON.

[0018] <u>Drawing 3</u> shows the example of a configuration of an arithmetic unit 2. This example of a configuration is equipped with CPU61, and this CPU61 is made as [compute / the new circuitry of PLD1] according to evaluation of actuation of the robot into which a designer 21 operates and inputs an input device 3 according to various processings, for example, the program of GA, according to the program memorized by ROM62. RAM63 is made as [memorize / CPU61 turns various processings up and / required data, a program, etc. / suitably].

[0019] Evaluation of actuation of the robot 11 which the designer 21 inputted is inputted through an interface 64 from an input unit 3. Moreover, the output of the control signal over PLD1 is also

performed through an interface 64.

[0020] Next, actuation of the above-mentioned example is explained with reference to the flow chart of drawing 4.

[0021] First, in step S1, an arithmetic unit 2 creates a predetermined number of syntax Ruhr. As shown in <u>drawing 5</u>, each syntax Ruhr has the one alphabet in left part, and has 2x2 matrices each element of whose is the alphabet in the right-hand side. An arithmetic unit 2 creates a gene from this syntax Ruhr, and uses as a chromosome that with which only the predetermined number connected the gene. An arithmetic unit 2 generates a predetermined number of initial chromosomes.

[0022] For example, when using the Ruhr 1 of <u>drawing 5</u> (a) as a gene, the Ruhr 1 is expressed as AOCHL. therefore — for example, when the chromosome which expresses the Ruhr 1 of <u>drawing 5</u> (a), the Ruhr 2 of <u>drawing 5</u> (b), and the Ruhr 3 of <u>drawing 5</u> (c) with a gene, and starts with these genes is described, it is shown in <u>drawing 6</u> — as — AOCHLFKHLKHTQJT — it becomes ... thus, the chromosome of predetermined die length — predetermined number creation — it carries out.

[0023] Next, in step S2, the matrix of the alphabet which has the magnitude corresponding to the number of the logic cell 41–1 in PLD1 thru/or 41–N is generated using these syntax Ruhr. For example, as shown in drawing 7 (a), first, the one alphabet (O) is set up, the syntax Ruhr 4 which has this alphabet (O) in left part, for example, the Ruhr shown in drawing 5 (d), is applied, and the alphabet (O) is changed into 2x2 matrix shown in drawing 7 (b). Next, this 2x2 matrix is changed into 4x4 matrix shown in drawing 7 (c) by applying the syntax Ruhr (not shown) which has these alphabet in left part to each elements Q, O, T, and E of this 2x2 matrix.

[0024] It becomes 8x8 matrix which similarly is shown in drawing 7 (d) when the syntax Ruhr is applied to each element of this 4x4 matrix, and further, if the syntax Ruhr is applied to the element of this matrix, it will become 16x16 matrix of drawing 7 (e). Thus, the syntax Ruhr is applied to each component of a matrix until the number of the lines in the matrix of the alphabet (= the number of trains) becomes more than the number of the logic cell 41-1 in PLD1 thru/or 41-N. Therefore, the matrix of the large-scale alphabet can also be created only in a predetermined number of syntax Ruhr.

[0025] For example, when the number of a logic cell 41-1 thru/or 41-N is 16 (N= 16), the magnitude of the matrix shown in <u>drawing 7</u> (e) is enough, the matrix of this alphabet is changed and the logical circuit incidence matrix which expresses the function which each logic cell performs as the integrated state of a logic cell is created.

[0026] The diagonal element of a logical circuit incidence matrix expresses the function of a logic cell 41–1 thru/or 41–N, and the component of the upper right one half of a logical circuit incidence matrix expresses the integrated state of a logic cell 41–1 thru/or 41–N. For example, when the i–th line of a logical circuit incidence matrix and the component of the j–th train are expressed with Aij and there is a function of a logic cell 41–1 thru/or 41–N by six all as shown in drawing 8, a diagonal element Aii is made into the integer of 0 thru/or 5, and expresses the i–th function (AND logical operation, OR logical operation, etc.) of logic-cell 41–i.

[0027] Moreover, the non-diagonal element Aij is set to 0 or 1, and expresses the i-th logic-cell 41-i and j-th integrated state of logic-cell 41-j. It means that logic-cell 41-i and logic-cell 41-j combine Aij when it is Aij=1, and when it is Aij=0, Aij means that such logic-cell 41-i and 41-j have not joined together. Therefore, an integrated state can be expressed only of the component of the upper right one half of this matrix, or lower left one half. In this example of a configuration, the component of the upper right one half of a matrix is used.

[0028] Next, in order to create this logical circuit incidence matrix, it changes into an alphabetical order from A about the diagonal element of the matrix of the alphabet either 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, ..., 0 or 5, and the other alphabet is changed into A, B, and C0 from the matrix of the alphabet as shown in drawing 7 (e) about a non-diagonal element 1. It is convertible for the logical circuit incidence matrix which shows the matrix of the alphabet shown in drawing 7 R> 7 (e) by this to drawing 8.

[0029] Thus, an arithmetic unit 2 generates a logical circuit incidence matrix from the set of the syntax Ruhr, and outputs it to PLD1 by making this matrix into a control signal. PLD1 changes

circuitry (the function and integrated state of a logic cell 41-1 thru/or 41-N) according to this control signal.

[0030] Next, in step S3, PLD1 operates a robot 11 according to the logical circuit set up at step S2. In step S4, the designer 21 who observed actuation of this robot 11 evaluates that actuation according to the predetermined evaluation approach, operates an input unit 3, and inputs that evaluation into an arithmetic unit 2.

[0031] When actuation which judges whether the robot 11 performed actuation which a designer 21 satisfies, and a designer 21 satisfies is performed from the evaluation whose designer 21 inputted the arithmetic unit 2 in step S5, processing is ended, and when the designer 21 is not satisfied, it progresses to step S6.

[0032] In step S6, after repeating processing of step S2 thru/or step S5 and completing these processings until it judges whether the robot 11 was operated corresponding to all chromosomes and operates a robot 11 about all chromosomes, it progresses to step S7.

[0033] And in step S7, based on GA, an arithmetic unit 2 performs three processings, selection processing, decussation processing, and mutation processing, and generates a next-generation chromosome from evaluation of the designer 21 to actuation of the robot 11 to each chromosome.

[0034] In selection processing, out of the ensemble of a chromosome, a chromosome is chosen by the probability proportional to evaluation of a designer 21, and the pair of a chromosome is built. Therefore, the probability which builds many pairs becomes high to the high (actuation of a robot 11 is realized) chromosome of evaluation, and the probability to leave many descendants to the next generation becomes high.

[0035] In decussation processing, it decides on the location which crosses two chromosomes by random numbers to each pair chosen by selection processing, and the value of all the digits after the digit is exchanged between two chromosomes. for example, the left to the 4th figure — Chromosome AOCHLFKHLK ... and Chromosome BTTDTCDMTP — the case where ... is made to cross — Chromosome BTTDLFKHLK ... and Chromosome AOCHTCDMTP — two chromosomes of ... are built.

[0036] In a chromosome, mutation processing is performed by a certain low fixed probability, when changing the alphabet of the digit determined by the random numbers and building a next-generation chromosome. When performing mutation processing, the digit to change is determined using a random number and the alphabet of the digit is changed. For example, in Chromosome JFAIEMJECP, when mutation occurs by the triple (alphabet A) figures from the left, the chromosome after processing serves as JFBIEMJECP.

[0037] It repeats after generating a next-generation chromosome until a designer 21 is satisfied with step S2 of processing of return, step S2, or step S7 in step S5 at actuation of a robot. [0038] The logical circuit which outputs the target signal is designed by updating the syntax Ruhr (chromosome) based on GA by using as a chromosome the set of the syntax Ruhr which derives the circuitry of PLD1 as mentioned above.

[0039] <u>Drawing 9</u> shows relation with the generation of the fitness and the chromosome in the case of solving an example of a MXOR (multiplex exclusive OR) problem in the circuit design circuit of this invention, and the one example of an approach. It is an index showing how close [to the output which the output of PLD which each chromosome expresses turns into at a target] fitness is. This MXOR problem makes it a technical problem to realize relation between the input of a logical circuit, and an output (16 inputs, eight outputs) which consists of eight XOR logical elements using PLD which has 64 logic cells.

[0040] A predetermined input is performed to PLD, and the function of PLD is updated using GA so that the difference of the output of PLD to this input and the output (the solution in question) at the time of using eight XOR may become small.

[0041] In this example, when at least the 95th generation uses the circuit design equipment of this invention, and one example of an approach to fitness being 750 (maximum) when a Prior art is used, it is the 10th generation, and the chromosome expressing the circuitry from which fitness is set to 780 appears, and a circuit design can be performed quickly.

[0042] Drawing 10 is the circuit design equipment of this invention, and one example of an

approach, and shows relation with the generation of the fitness and the chromosome in the case of solving an example of 6 multiplexer (6-Multiplexor) problem.

[0043] Six multiplexers have four input channels, two multiplexer signal channels, and one output channel, and output the value of one of four input channels to an output channel according to the value of a multiplexer signal channel. Six multiplexer problems make it a technical problem to realize relation between the input of these six multiplexers, and an output.

[0044] In this example, the input corresponding to four input channels and two multiplexer signal channels is performed to PLD, and the function of PLD is updated using GA so that the difference of the output of PLD to this input and the output (the solution in question) of six actual multiplexers may become small.

[0045] When at least the 45th generation uses the circuit design equipment of this invention, and one example of an approach to fitness being 0.66 (maximum) when a Prior art is used, by the 5th generation, the chromosome expressing the circuitry from which fitness is set to 0.98 appears, and a circuit design can be performed quickly.

[0046] In addition, in the above example, although a robot's 11 control circuit was designed, this invention is applicable also to the design of a general logical circuit.

[0047] In the above-mentioned example, although the whole region of a logical circuit was designed using GA, the logical circuit already designed can be changed into the syntax Ruhr, and the logical circuit can also be used as a part of newly designed logical circuit by including the syntax Ruhr in the chromosome of GA. In this case, to the syntax Ruhr incorporated, the decussation processing and mutation processing in GA are not performed, but a logical circuit [finishing / that design] is included in the newly designed logical circuit. [0048]

[Effect of the Invention] As mentioned above, since according to circuit design equipment according to claim 1 and the circuit design approach according to claim 2 the result of an operation changed the calculation function based on the genetic algorithm which uses as a chromosome the syntax Ruhr which derives a calculation function so that the target value might be approached, the die length of a chromosome is proportional to the number of the syntax Ruhr, and since it is not dependent on the scale of a logical circuit, a large-scale logical circuit can be designed quickly and easily.

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.*** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the example of a configuration of one example of the circuit design equipment of this invention.

[Drawing 2] It is the block diagram showing the example of a configuration of PLD1 in the example of drawing 1.

[Drawing 3] It is the block diagram showing the example of a configuration of the arithmetic unit 2 in the example of $\frac{1}{2}$.

[Drawing 4] It is a flow chart explaining actuation of the example of drawing 1.

[Drawing 5] It is drawing showing the example of the syntax Ruhr used in the example of drawing

[Drawing 6] It is drawing showing the example of the chromosome used in the example of drawing 1.

[Drawing 7] It is drawing showing the example which develops a matrix according to the syntax Ruhr as shown in drawing 5.

[Drawing 8] It is drawing showing the example of the logical circuit incidence matrix drawn in the example of drawing 1.

[Drawing 9] It is drawing showing relation with the generation of the fitness and the chromosome when solving an example of a MXOR problem with the application of one example of this invention.

[Drawing 10] It is drawing showing relation with the generation of the fitness and the chromosome when solving an example of 6 multiplexer problems with the application of one example of this invention.

[Description of Notations]

- 1 PLD
- 2 Arithmetic Unit
- 3 Input Unit
- 11 Robot
- 21 Designer
- 41-1 thru/or 41-N Logic cell
- 42-1 thru/or 42-M Joint switch
- 61 CPU
- 62 ROM
- **63 RAM**
- 64 Interface

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.*** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law

[Section partition] The 3rd partition of the 6th section [Publication date] December 20, Heisei 14 (2002. 12.20)

[Publication No.] JP,9-81615,A

[Date of Publication] March 28, Heisei 9 (1997. 3.28)

[Annual volume number] Open patent official report 9-817

[Application number] Japanese Patent Application No. 7-236512

[The 7th edition of International Patent Classification]

G06F 17/50 15/18 550

[FI]

G06F 15/60 654 D 15/18 550 C

[Procedure revision]

[Filing Date] September 17, Heisei 14 (2002. 9.17)

[Procedure amendment 1]

[Document to be Amended] Specification

[Item(s) to be Amended] Claim

[Method of Amendment] Modification

[Proposed Amendment]

[Claim(s)]

[Claim 1] An operation means by which it can calculate and a calculation function can be

changed dynamically,

Circuit design equipment characterized by having the control means which changes said calculation function so that the output of said operation means may approach the output of the purpose based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives said calculation function.

[Claim 2] Said control means is circuit design equipment according to claim 1 characterized by creating said chromosome by combining said two or more syntax Ruhr.

[Claim 3] Said syntax Ruhr is circuit design equipment according to claim 2 characterized by consisting of combination of the 1st element and the 2nd element.

[Claim 4] Said 1st element consists of one element, and said 2nd element consists of two or more elements,

Said control means is circuit design equipment according to claim 3 which is repeating the processing which assumes each of two or more of said 2nd elements as said 1st element, and transposes it to said 2nd element corresponding to said the 1st assumed element, and is

characterized by creating the matrix of said element.

[Claim 5] Circuit design equipment according to claim 4 characterized by making the diagonal element of said matrix correspond to each function of two or more cels which constitute said operation means, and making non-diagonal elements other than said diagonal element correspond to the integrated state of said cel.

[Claim 6] The circuit design approach characterized by changing said calculation function so that the result of said operation may approach the target value based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives said calculation function of the arithmetic element which calculates, and which can change a calculation function dynamically. [Claim 7] The circuit design approach according to claim 6 characterized by creating said

chromosome by combining said two or more syntax Ruhr.

[Claim 8] Said syntax Ruhr is the circuit design approach according to claim 7 characterized by consisting of combination of the 1st element and the 2nd element.

[Claim 9] Said 1st element consists of one element, and said 2nd element consists of two or more elements,

The circuit design approach according to claim 8 characterized by creating the matrix of said element by repeating the processing which assumes each of two or more of said 2nd elements as said 1st element, and transposes it to said 2nd element corresponding to said the 1st assumed element.

[Claim 10] The circuit design approach according to claim 9 characterized by making the diagonal element of said matrix correspond to each function of two or more cels which constitute said arithmetic element, and making non-diagonal elements other than said diagonal element correspond to the integrated state of said cel.

[Procedure amendment 2]

[Document to be Amended] Specification

[Item(s) to be Amended] 0009

[Method of Amendment] Modification

[Proposed Amendment]

[0009]

[Means for Solving the Problem] Circuit design equipment according to claim 1 calculates, and is characterized by having an operation means by which a calculation function can be changed dynamically, and the control means which changes a calculation function so that the output of an operation means may approach the output of the purpose based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives a calculation function. Said control means can create a chromosome by combining two or more syntax Ruhr. Said syntax Ruhr can consist of combination of the 1st element and the 2nd element. The matrix of an element can be created by said 1st element consisting of one element, and the 2nd element consisting of two or more elements, and repeating the processing whose control means assumes each of two or more 2nd elements as the 1st element, and transposes it to the 2nd element corresponding to the 1st assumed element. The diagonal element of said matrix is made to correspond to each function of two or more cels which constitute an operation means, and non-diagonal elements other than a diagonal element can be made to correspond to the integrated state of a cel.

[Procedure amendment 3]

[Document to be Amended] Specification

[Item(s) to be Amended] 0010

[Method of Amendment] Modification

[Proposed Amendment]
 [0010] The circuit design approach according to claim 6 is characterized by changing said calculation function so that the result of said operation may approach the target value based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives said calculation function of the arithmetic element which calculates, and which can change a calculation function dynamically. A chromosome can be created by combining two or more syntax Ruhr. Said syntax Ruhr can consist of combination of the 1st element and the 2nd element. Said 1st element can consist of one element, the 2nd element can consist of two or more elements, each of two or more 2nd elements can be

assumed as the 1st element, and the matrix of an element can be created by repeating processing replaced with the 2nd element corresponding to the 1st assumed element. The diagonal element of said matrix is made to correspond to each function of two or more cels which constitute an arithmetic element, and non-diagonal elements other than a diagonal element can be made to correspond to the integrated state of a cel.

[Procedure amendment 4]

[Document to be Amended] Specification

[Item(s) to be Amended] 0011

[Method of Amendment] Modification

[Proposed Amendment]

[0011] In circuit design equipment according to claim 1, an operation means by which a calculation function can be changed dynamically calculates, and a control means changes a calculation function so that the output of an operation means may approach the output of the purpose based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives a calculation function.

[Procedure amendment 5]

[Document to be Amended] Specification

[Item(s) to be Amended] 0012

[Method of Amendment] Modification

[Proposed Amendment]

[0012] In the circuit design approach according to claim 6, said calculation function is changed so that the result of said operation may approach the target value based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives said calculation function of the arithmetic element which calculates, and which can change a calculation function dynamically.

[Procedure amendment 6]

[Document to be Amended] Specification

[item(s) to be Amended] 0048

[Method of Amendment] Modification

[Proposed Amendment]

[0048]

[Effect of the Invention] As mentioned above, since according to circuit design equipment according to claim 1 and the circuit design approach according to claim 6 the calculation function was changed so that the result of an operation might approach the target value based on the genetic algorithm which generates a chromosome from the syntax Ruhr which derives a calculation function, the die length of a chromosome is proportional to the number of the syntax Ruhr, and since it is not dependent on the scale of a logical circuit, a large-scale logical circuit can be designed quickly and easily.

(19)日本国特許庁 (JP) (12) 公開特許公報 (A)

(11)特許出顧公開番号

特開平9-81615

(43)公開日 平成9年(1997)3月28日

(51) Int.Cl. ⁶	識別記号	庁内整理番号	FΙ		技術表示箇所		
G06F 17/50	0		G06F 1		654D		
15/18	8 550		1	5/18	5 5 0 C		
			審査請求	未請求。請求以	質の数2 OL	(全 7 頁)	
(21) 出顧番号 特願平7-23			(71)出顧人		000002185		
(22)出顧日	平成7年(1995)9月14日			東京都品川区は	比品川6丁目7	番35号	
					東京都品川区北品川6丁目7番35号 ソニ		
			(74)代理人	一株式会社内 弁理士 稲本	義雄		
(54)【発明の名称] 回路設計装置およ	び方法					
(57)【要約】 【課題】 大規模な論理回路を設計することができるようにする。 【解決手段】 遺伝的アルゴリズムに基づいて、プログラム可能な論理回路(PLD: Programmable Logic Device)の回路構成を更新し、目的の出力を行う論理回路を設計する。遺伝的アルゴリズムに従って、PLDの回路構成を導出する文法ルール(例えば、図5(a)乃至			(a)	ルール 1	A →	O C H L	
			(b)	ルール2	F ->	[к н] L к]	
図5 (d))の集合を染色体とし、この染色体(文法ルールの集合)を更新していき、最適な回路構成を与える染色体を導出する。このとき、染色体の長さは、文法ルールの数に比例するので、PLDの回路の規模に依存せず、PLDの回路が大規模である場合でも、適度な計算時間で、回路構成の設計を行うことができる。		D染色体(文法ル 回路構成を与える D長さは、文法ル	(c)	ルール3	Н ->-	[т Q] [л т]	
		(d)	JレーJレ 4	0 ->	Q O T E		

【特許請求の範囲】

【請求項1】 演算を行い、動的に演算機能を変更することができる演算手段と、

前記演算機能を導出する文法ルールを染色体とする遺伝 的アルゴリズムに基づいて、前記演算手段の出力が目的 の出力に近づくように、前記演算機能を変更する制御手 段とを備えることを特徴とする回路設計装置。

【請求項2】 演算を行う、動的に演算機能を変更することができる演算素子の前記演算機能を導出する文法ルールを染色体とする遺伝的アルゴリズムに基づいて、前記演算の結果が目的の値に近づくように、前記演算機能を変更することを特徴とする回路設計方法。

【発明の詳細な説明】

[0001]

【発明の属する技術分野】本発明は、回路設計装置および方法に関し、特に、遺伝的アルゴリズムに基づいて、 回路構成を変更していく回路設計装置および方法に関する。

[0002]

【従来の技術】従来、設計者は、ロボットなどを制御する複雑な論理回路を設計する場合、多くの基本的な論理素子を経験的に組み合わせて、論理回路を設計していた。しかしながら、最近では、遺伝的アルゴリズム(GA: Genetic Algorithm)に基づいて、経験的な知識を必要とせずに論理回路を設計する方法が、例えば、樋口氏らによって、「遺伝的アルゴリズム(北野宏明編、産業図書)」において、「遺伝的学習によるハードウェア進化の基礎実験」として紹介されている。

【OOO3】この方法においては、FPGA(Field Programmable Gate Array)に代表される、プログラム可能な論理回路(PLD: Programmable Logic Device)の回路構成を、GAに基づいて繰り返し変更し、目的の出力を行う論理回路を作成する。

【0004】PLDは、AND論理演算、OR論理演算などの基本的な論理計算の種類を動的に選択することができる論理セルを複数個有し、各論理セルが実行する論理計算の種類と、これらの論理セル間の回路結合のパターンを変更することができる。

【0005】GAにおいては、最適化する対象を特徴づけるものが遺伝子で表現され、この遺伝子を連結することで、染色体が生成される。そして、複数の染色体を繰り返し更新することで、対象を最適な状態へ近づけていく。

【0006】従来、PLDにおける論理セルの機能と論理セル間の回路結合のパターンが、染色体で表現され、この染色体(PLDの回路構成)をGAに基づいて更新していき、目的の出力を行う論理回路を作成するようになされている。

[0007]

【発明が解決しようとする課題】しかしながら、複雑な

制御を行う論理回路を設計する場合、多数の論理演算素子が必要とされ、これらの論理演算素子間の結合パターンも複雑になる。従来の技術では、PLDにおける論理セルの機能と回路結合のパターンを染色体で表現するため、染色体の長さは、論理セルの数に応じて長くなる。従って、大規模な論理回路を設計する場合、非常にした、まで、多くの計算時間を要するという課題を有している。【0008】本発明は、このような状況に鑑みてないたもので、所定の数の文法ルールからなる文法ルールの集合で、論理セルの機能と結合パターンを生成し、これらの文法ルールを染色体で表現することで、染色体の良きを論理セルの数に依存しないようにし、大規模な論理回路を設計できるようにするものである。

[0009]

【課題を解決するための手段】請求項1に記載の回路設計装置は、演算を行い、動的に演算機能を変更することができる演算手段と、演算機能を導出する文法ルールを染色体とする遺伝的アルゴリズムに基づいて、演算手段の出力が目的の出力に近づくように、演算機能を変更する制御手段とを備えることを特徴とする。

【〇〇1〇】請求項2に記載の回路設計方法は、演算を行う、動的に演算機能を変更することができる演算案子の前記演算機能を導出する文法ルールを染色体とする遺伝的アルゴリズムに基づいて、前記演算の結果が目的の値に近づくように、前記演算機能を変更することを特徴とする。

【〇〇11】請求項1に記載の回路設計装置においては、動的に演算機能を変更することができる演算手段は、演算を行い、制御手段は、演算機能を導出する文法ルールを染色体とする遺伝的アルゴリズムに基づいて、演算手段の出力が目的の出力に近づくように、演算機能を変更する。

【0012】請求項2に記載の回路設計方法においては、演算を行う、動的に演算機能を変更することができる演算素子の前記演算機能を導出する文法ルールを染色体とする遺伝的アルゴリズムに基づいて、前記演算の結果が目的の値に近づくように、前記演算機能を変更する。

[0013]

【発明の実施の形態】図1は、本発明の回路設計装置の一実施例の構成例を示している。この構成例は、PLD1(演算手段)を備える。PLD1は、演算装置2(制御手段)に接続され、演算装置2の制御信号に従って、その回路構成を変更し、その回路構成で、ロボット11に制御信号を出力するようになされている。

【0014】ロボット11は、PLD1から供給される制御信号に従って、動作を行うようになされている。設計者21は、ロボット11の動作を観察し、所定の評価方法(評価関数)に従って、その動作の評価を行い、入

カ装置3を操作して演算装置2に、その評価に対応する 入力を行う。

【0015】演算装置2は、所定の数の染色体を保持し、各染色体から、PLD1の回路構成を導出して、制御信号としてPLD1に出力するようになされている。また、すべての染色体について、ロボット11の動作と設計者21の評価が終了した後、演算装置2は、GAに基づいて、評価が高い動作を実現した回路構成に対応する染色体の子孫が次世代に多く残る確率を高くして、染色体を更新するようになされている。

【〇〇16】図2は、PLD1の構成例を示している。この構成例は、複数の論理セル41-1乃至41-Nを備える。これらの論理セル41-1乃至41-Nは、AND論理演算、OR論理演算などの複数の基本的な論理計算機能を有し、外部から供給される制御信号に従って、動的に、実行する論理計算の種類を変更するようになされている。

【0017】論理セル41-1万至41-Nは、どの論理セル同士でも結合することができるようになされており、それぞれの論理セル間を結合するか否かは、外部から供給される制御信号で決定される。論理セル間を結合する場合は、結合スイッチ42-1万至42-Mのうちの対応する結合スイッチをオンにする。例えば、論理セル41-Nと論理セル41-1とを結合する場合、結合スイッチ42-1をオンにする。

【0018】図3は、演算装置2の構成例を示している。この構成例は、CPU61を備え、このCPU61は、ROM62に配憶されているプログラムに従って、各種処理、例えば、GAのプログラムに従って、設計者21が入力装置3を操作して入力するロボットの動作の評価に応じて、PLD1の新たな回路構成を算出するようになされている。RAM63は、CPU61が各種処理をする上において必要なデータ、プログラムなどを適宜記憶するようになされている。

【0019】設計者21が入力したロボット11の動作の評価は、入力装置3からインターフェース64を介して入力される。また、PLD1に対する制御信号の出力も、インターフェース64を介して行われる。

【0020】次に、図4のフローチャートを参照して、 上記実施例の動作について説明する。

【0021】最初に、ステップS1において、演算装置2は、所定の数の文法ルールを作成する。図5に示すように、各文法ルールは、左辺に1個のアルファベットを有し、右辺に各要素がアルファベットである2×2行列を有する。演算装置2は、この文法ルールから遺伝子を作成し、遺伝子を所定の数だけ連結したものを染色体とする。演算装置2は、所定の数の初期染色体を生成する

【0022】例えば、図5(a)のルール1を遺伝子とする場合、ルール1は、AOCHLと表現される。従っ

て、例えば、図5 (a) のルール1、図5 (b) のルール2、および図5 (c) のルール3を遺伝子で表現し、これらの遺伝子で始まる染色体を記述すると、図6に示すように、AOCHLFKHLKHTQJT・・・となる。このようにして、所定の長さの染色体を、所定の数作成する。

【0023】次に、ステップS2において、これらの文法ルールを利用して、PLD1における論理セル41-1乃至41-Nの数に対応する大きさを有するアルファベットの行列を生成する。例えば、図7(a)に示すように、最初に、1個のアルファベット(O)を設定し、左辺にこのアルファベット(O)を有する文法ルール、例えば、図5(d)に示すルール4を適用して、アルファベット(O)を図7(b)に示す2×2行列に変換する。次に、この2×2行列の各要素Q、O、T、およびEに対して、左辺にこれらのアルファベットを有する文法ルール(図示せず)を適用することで、この2×2行列は、図7(c)に示す4×4行列に変換される。

【0024】同様に、この4×4行列の各要素に文法ルールを適用すると、図7(d)に示す8×8行列になり、さらに、この行列の要素に文法ルールを適用すると、図7(e)の16×16行列となる。このようにして、アルファベットの行列における行の数(=列の数)が、PLD1における論理セル41-1乃至41-Nの数以上になるまで、行列の各成分に文法ルールを適用する。従って、所定の数の文法ルールだけで、大規模なアルファベットの行列を作成することもできる。

【OO25】例えば、論理セル41-1乃至41-Nの数が16(N=16)である場合、図7(e)に示す行列の大きさで充分であり、このアルファベットの行列を変換して、論理セルの結合状態と、各論理セルが実行する機能を表す論理回路結合行列を作成する。

【0026】論理回路結合行列の対角成分は、論理セル41-1乃至41-Nの機能を表し、論理回路結合行列の右上半分の成分は、論理セル41-1乃至41-Nの結合状態を表現する。例えば、論理回路結合行列の第i行、第i列の成分をAijで表すと、図8に示すように、論理セル41-1乃至41-Nの機能が全部で6個ある場合、対角成分Aiiは、O乃至5の整数とし、第i番目の論理セル41-iの機能(AND論理演算、OR論理演算など)を表現する。

【〇〇27】また、非対角成分Aijは、〇もしくは1とし、第i番目の論理セル41-iと第j番目の論理セル41-jの結合状態を表現する。Aij=1である場合、Aijは、論理セル41-iと論理セル41-jが結合することを表し、Aij=0である場合、Aijは、これらの論理セル41-i 41-jが結合していないことを表す。従って、この行列の右上半分もしくは左下半分の成分だけで結合状態を表現することができる。この構成例においては、行列の右上半分の成分を利

用している。

【〇〇28】次に、図7(e)に示すようなアルファベットの行列から、この論理回路結合行列を作成するには、例えば、アルファベットの行列の対角成分について、Aからアルファベット順に、〇. 1. 2. 3. 4. 5. 0. 1. 2. 3. ・・・と、〇乃至5のいずれかに変換し、非対角成分については、A. B. Cを〇に、その他のアルファベットを1に変換する。これにより、図7(e)に示すアルファベットの行列を、図8に示す論理回路結合行列に変換することができる。

【0029】このようにして、演算装置2は、文法ルールの集合から論理回路結合行列を生成し、この行列を制御信号として、PLD1に出力する。PLD1は、この制御信号に従って、回路構成(論理セル41-1乃至41-Nの機能および結合状態)を変更する。

【0030】次にステップS3において、PLD1は、ステップS2で設定した論理回路に従って、ロボット11を動作させる。このロボット11の動作を観察した設計者21は、ステップS4において、その動作を所定の評価方法に従って評価し、入力装置3を操作して、その評価を演算装置2に入力する。

【0031】ステップS5において、演算装置2は、設計者21が入力した評価から、設計者21が満足する動作をロボット11が行ったか否かを判断し、設計者21が満足する動作を行った場合は、処理を終了し、設計者21が満足していない場合、ステップS6に進む。

【0032】ステップS6においては、すべての染色体に対応して、ロボット11を動作させたか否かを判断し、すべての染色体についてロボット11を動作させるまで、ステップS2乃至ステップS5の処理を繰り返し、これらの処理が終了した後、ステップS7に進む。【0033】そして、ステップS7において、演算装むとは、各染色体に対するロボット11の動作に対する設計者21の評価から、GAに基づいて、選択処理、交叉処理、突然変異処理の3つの処理を行い、次世代の染色体を生成する。

【0034】選択処理においては、染色体の集団の中から、設計者21の評価に比例した確率で染色体を選択して、染色体のペアをつくる。従って、評価の高い(ロボット11の動作を実現する)染色体に対して、多くのペアをつくる確率が高くなり、次世代に多くの子孫を残す確率が高くなる。

【0035】交叉処理においては、選択処理で選択された各ペアに対して、乱数で2つの染色体を交叉する場所を決定し、その桁以降のすべての桁の値を、2個の染色体の間で交換する。例えば、左から4桁目で染色体AOCHLFKHLK・・・と染色体BTTDLFKHLK・・・と、染色体AOCHTCDMTP・・・の2個の染色体がつくられる。

【0036】突然変異処理は、染色体において、乱数で決定した桁のアルファベットを変化させるもので、次世代の染色体をつくるとき、ある一定の低い確率で行われる。突然変異処理を行う場合は、変化させる桁を乱数を用いて決定し、その桁のアルファベットを変更する。例えば、染色体JFAIEMJECPにおいて、左から3桁目(アルファベットA)で突然変異が起きた場合、処理後の染色体は、例えば、JFBIEMJECPとなる。

【0037】次世代の染色体を生成した後、ステップS2に戻り、ステップS2乃至ステップS7の処理を、ステップS5において設計者21が、ロボットの動作に満足するまで繰り返す。

【0038】以上のようにして、PLD1の回路構成を 導出する文法ルールの集合を染色体として、GAに基づ いて文法ルール(染色体)を更新することで、目的の信 号を出力する論理回路を設計する。

【0039】図9は、本発明の回路設計回路および方法の一実施例でMXOR(多重排他的論理和)問題の一例を解く場合の、適応度と染色体の世代との関係を示している。適応度は、各染色体が表現するPLDの出力が、目標となる出力にどの程度近いかを表す指標である。このMXOR問題は、64個の論理セルを有するPLDを用いて、8個のXOR論理素子から構成される論理回路の入力と出力の関係(16入力、8出力)を実現することを課題とする。

【OO40】PLDに所定の入力を行い、この入力に対するPLDの出力と、8個のXORを用いた場合の出力(問題の解)との差が小さくなるように、GAを用いて、PLDの機能を更新していく。

【0041】この例においては、従来の技術を用いた場合、95世代目でも適応度が750(最大値)であるのに対して、本発明の回路設計装置および方法の一実施例を用いた場合、10世代目で、適応度が780となる回路構成を表現する染色体が現れ、迅速に回路設計を行うことができる。

【0042】図10は、本発明の回路設計装置および方法の一実施例で、6マルチプレクサ(6-Multiplexor)問題の一例を解く場合の、適応度と染色体の世代との関係を示している。

【0043】6マルチプレクサは、4つの入力チャンネルと、2つのマルチプレックス信号チャンネルと、1つの出力チャンネルを有し、マルチプレックス信号チャンネルの値に従って、4つのうちの1つの入力チャンネルの値を出力チャンネルに出力する。6マルチプレクサ問題は、この6マルチプレクサの入力と出力との関係を実現することを課題とする。

【0044】この例においては、PLDに4つの入力チャンネルと、2つのマルチプレックス信号チャンネルに対応する入力を行い、この入力に対するPLDの出力

と、実際の6マルチプレクサの出力(問題の解)との差が小さくなるように、GAを用いて、PLDの機能を更新していく。

【0045】従来の技術を用いた場合、45世代目でも 適応度が0.66(最大値)であるのに対して、本発明 の回路設計装置および方法の一実施例を用いた場合、5 世代目で、適応度が0.98となる回路構成を表現する 染色体が現れ、迅速に回路設計を行うことができる。

【0046】なお、以上の実施例においては、ロボット 11の制御回路を設計したが、一般の論理回路の設計に も、本発明を適用することができる。

【0047】上記実施例において、GAを利用して、論理回路の全域を設計したが、既に設計されている論理回路を文法ルールに変換し、その文法ルールをGAの染色体に組み込むことで、その論理回路を、新たに設計する論理回路の一部として利用することもできる。この場合、組み込まれる文法ルールに対しては、GAにおける交叉処理と突然変異処理を行わず、その設計済みの論理回路が、新たに設計する論理回路に組み込まれるようにする。

[0048]

【発明の効果】以上のように、請求項1に記載の回路設計装置および請求項2に記載の回路設計方法によれば、演算機能を導出する文法ルールを染色体とする遺伝的アルゴリズムに基づいて、演算の結果が、目的の値に近づくように、演算機能を変更するようにしたので、染色体の長さは、文法ルールの数に比例し、論理回路の規模には依存しないので、大規模な論理回路を迅速かつ簡単に設計することができる。

【図面の簡単な説明】

【図1】本発明の回路設計装置の一実施例の構成例を示すブロック図である。

【図2】図1の実施例におけるPLD1の構成例を示す ブロック図である。

【図3】図1の実施例における演算装置2の構成例を示すブロック図である。

【図4】図1の実施例の動作を説明するフローチャート である。

【図5】図1の実施例で利用される文法ルールの例を示す図である。

【図6】図1の実施例で利用される染色体の例を示す図である。

【図7】図5に示すような文法ルールに従って、行列を 展開する例を示す図である。

【図8】図1の実施例において導出される論理回路結合 行列の例を示す図である。

【図9】本発明の一実施例を適用してMXOR問題の一例を解いたときの、適応度と染色体の世代との関係を示す図である。

【図10】本発明の一実施例を適用して6マルチプレク サ問題の一例を解いたときの、適応度と染色体の世代と の関係を示す図である。

【符号の説明】

1 PLD

2 演算装置

3 入力装置

11 ロボット

2 1 設計者

4.1-1乃至41-N 論理セル

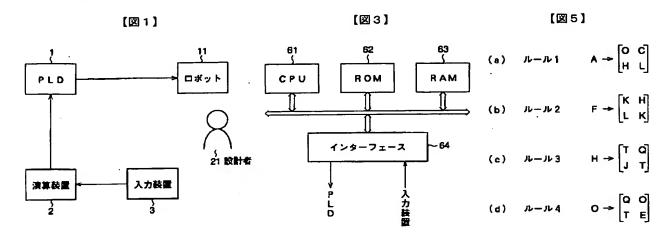
42-1乃至42-M 結合スイッチ

61 CPU

62 ROM

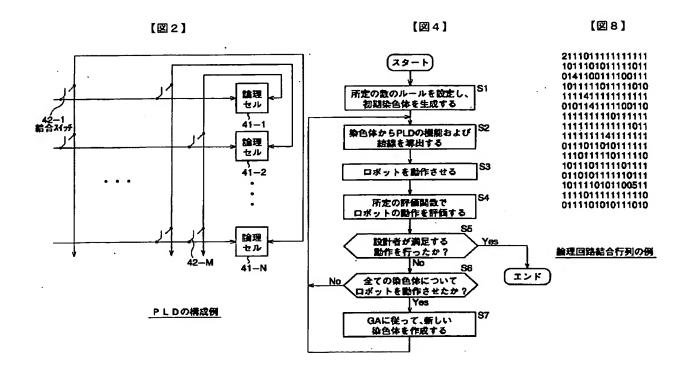
63 RAM

64 インターフェース



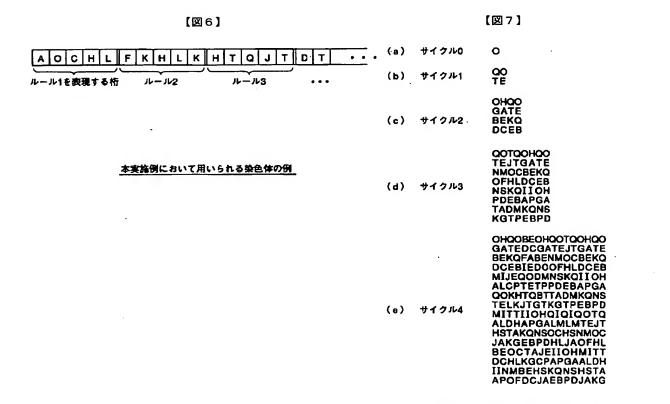
本発明の回路設計装置の実施例の構成例

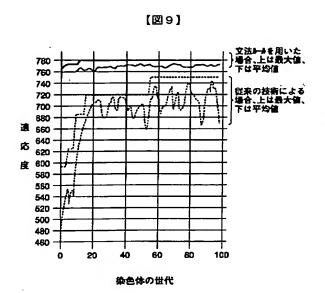
演算装置の構成例

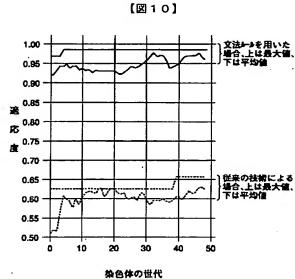


本発明の回路設定装置の実施例の処理例

ルールを適用して所定の大きさの行列を作成するの例







MXOR問題における適応度と染色体の世代との関係

6マルチプレクサ問題における適応度と染色体の世代との関係